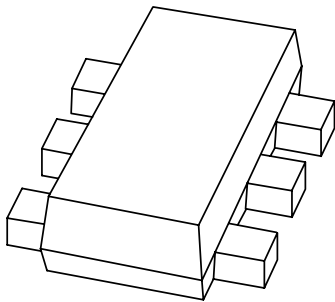


# DATA SHEET



## **PBSS5140V** 40 V low $V_{CEsat}$ PNP transistor

Product specification  
Supersedes data of 2001 Oct 19

2002 Mar 20

# 40 V low $V_{CEsat}$ PNP transistor

# PBSS5140V

### FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm × 1.2 mm × 0.55 mm ultra thin package
- Improved thermal behaviour due to flat leads
- Self alignment during soldering due to straight leads
- Low collector-emitter saturation voltage
- High current capability

### APPLICATIONS

- General purpose switching and muting
- LCD back lighting
- Supply line switching circuits
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

### DESCRIPTION

PNP low  $V_{CE sat}$  transistor in a SOT666 plastic package.  
NPN complement: PBSS4140V.

### MARKING

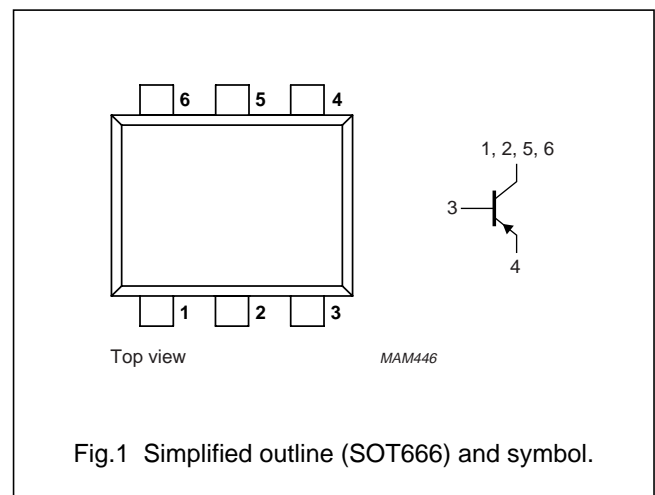
TYPE NUMBER	MARKING CODE
PBSS5140V	25

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	-40	V
$I_C$	collector current (DC)	-1	A
$I_{CM}$	peak collector current	-2	A
$R_{CEsat}$	equivalent on-resistance	<340	m $\Omega$

### PINNING

PIN	DESCRIPTION
1	collector
2	collector
3	base
4	emitter
5	collector
6	collector



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–1	A
$I_{CM}$	peak collector current		–	–2	A
$I_B$	base current (DC)		–	–300	mA
$I_{BM}$	peak base current		–	–1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	300	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	500	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single side copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	410	K/W
		note 2	215	K/W

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single side copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

**Soldering**

The only recommended soldering is reflow soldering.

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**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -40\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -40\text{ V}; I_E = 0; T_{amb} = 150\text{ °C}$	–	–	–50	$\mu\text{A}$
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; I_B = 0$	–	–	–100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -1\text{ mA}$	300	–	–	
		$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}$	300	–	800	
		$V_{CE} = -5\text{ V}; I_C = -500\text{ mA}$	250	–	–	
		$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	160	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	–80	–140	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–120	–170	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	–	–200	–310	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -500\text{ mA}; I_B = -50\text{ mA}; \text{note 1}$	–	240	<340	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	–	–	–1	V
$f_T$	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	150	–	–	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	12	pF

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .

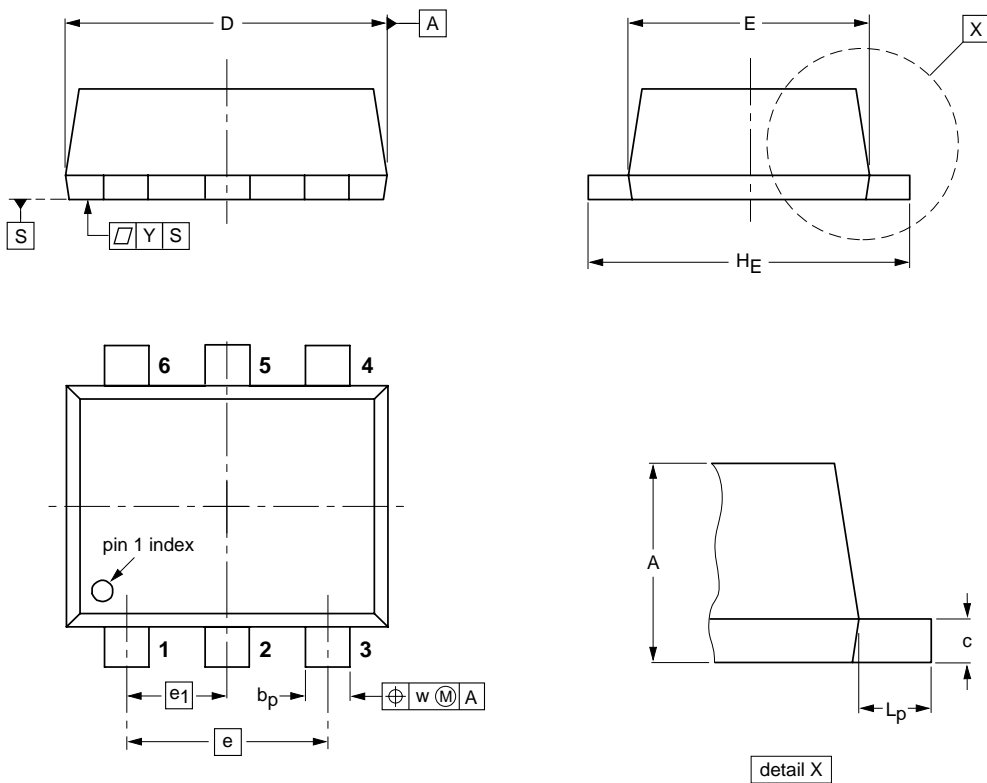
40 V low  $V_{CEsat}$  PNP transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						-01-01-04 01-08-27

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